REMARKS

Entry of this Amendment is proper because it does not raise any new issues requiring further search by the Examiner, narrows the issues on appeal, and is believed to place the present application in condition for immediate allowance.

Claims 1-4, 6, 9, 20, and 23-30 are presently pending in the application.

Claim 23 has been amended merely to make a minor editorial change (non-substantive).

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicants specifically state that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claim 20 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Damouny (U.S. Patent No. 4,713,750). Claims 1-4, 6, and 9 stand rejected under 35 U.S.C. § 103(s) as being unpatentable over Damouny in view of Thoma (U.S. Patent No. 4,484,268).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention relates to a microprocessor, a microcode unit in a microprocessor, and a method of providing a state machine decoding.

In the illustrative, non-limiting embodiment of the invention, as defined by independent claim 1, a microprocessor includes a microcode unit for outputting control signals, for each of a plurality of instructions, required by said microprocessor for executing said instructions. The microcode unit includes an instruction address input for receiving an instruction address, a

control variable input for receiving a control variable corresponding to a current state of the microprocessor, a control signal input for receiving all the control signals output by the microcode unit for an immediately preceding instruction, and a plurality of embedded logic circuits each dedicated for evaluating one unique type of instruction received by the microcode unit and for setting the control signals *required* for executing said received instruction.

In another exemplary embodiment of the present invention, as defined by independent claim 9, a microcode unit in a microprocessor, for outputting control signals, for each of a plurality of instructions, required by said microprocessor for executing said instructions, the microcode unit includes an instruction address input for receiving an instruction address, a control variable input for receiving a control variable corresponding to a current state of the microprocessor, a control signal input for receiving all the control signals output by the microcode unit for an immediately preceding instruction, and a plurality of embedded logic circuits each dedicated for evaluating one unique type of instruction received by the microcode unit and for setting the control signals *required* for executing said received instruction.

In another exemplary embodiment of the present invention, as defined by independent claim 20, a method of providing a state machine decoding includes decoding a current opcode to provide a decode, setting required functions signals, setting exclusive functions outside of the current opcode to a previous state; and latching results of the decode.

In the claimed invention, in addition to the "0" or "1" value which can be set for each control signal, the previous value can also be set, thereby reducing the power within the microprocessor (e.g., see specification at page 10, lines 2-5).

Specifically, since each function is a function of a microcode address, by only changing the value of control signals that are absolutely required for that particular microcode address

(e.g., ADD, STORE, MULT etc. as determined by the decoding), the power of the microprocessor can be minimized since node toggle, as discussed above, is greatly reduced as compared to the conventional machines and systems (e.g., see specification at page 10, lines 6-11).

For example, in an exemplary embodiment of the claimed invention, the power savings was on the order of about 30-40% over the conventional systems. Hence, if the function remains the same from a previous opcode to the next opcode (and hence from cycle-to-cycle), then the previous value may be maintained again, and no node toggle results since values are not being changed from high to low or from low to high (e.g., see specification at page 10, lines 11-16).

Thus, with the claimed invention, each opcode becomes a function of the previous opcode and only conflicting (e.g., required) control signals must be resolved, thereby greatly reducing power consumption (e.g., see specification at page 10, lines 17-19).

II. THE PRIOR ART REJECTIONS

The Examiner maintains the rejection of claim 20 under 35 U.S.C. § 102(b) as being anticipated by Damouny and the rejection of claims 1-4, 6, and 9 under 35 U.S.C. § 103(a) as being unpatentable over Damouny in view of Thoma.

For the following reasons, Applicants respectfully traverse these rejections.

For the Examiner's convenience, the traversal arguments set forth in the Amendment under 37 C.F.R. § 1.111 filed on July 16, 2004 are incorporated herein by reference in their entirety.

In the Response to Arguments, the Examiner alleges that "*the features upon which Applicant relies (i.e., that only the required control signals are resolved or changed) are not*

recited in the rejected claim(s)...since the claims read that the required control signals are changed, the reference must teach that these control signals are changed, but may also disclose other control signals that are changed since the claim mentions nothing about the other control signals" (see Office Action at page 13, numbered paragraph 24; emphasis added).

However, Applicants respectfully note that claim 24 clearly recites that "*each of the plurality of embedded logic circuits comprises a controller for controllably setting only each of the control signals required by the microprocessor for executing said received instruction*" (emphasis added). The rejection of claim 24 is addressed below.

In the Response to Arguments, the Examiner alleges that "*a recitation of intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim*" (see Office Action at page 14, numbered paragraph 25; emphasis added).

However, for the reasons set forth below, Applicants respectfully submit that, even if arguments of intended use have been asserted, the applied references are not capable of performing the intended use of the claimed invention, and indeed, do not disclose, suggest, or even mention the intended use and/or advantages of the claimed invention.

For the reasons set forth below, Applicants respectfully reiterate that Damouny and Thoma, either alone or in combination, do not disclose, suggest, or even mention these features of the claimed invention, or for that matter, the advantages derived from the unique combination of structural features recited in the claimed invention.

For example, as mentioned above, the claimed invention provides a novel and unique combination of elements in which, since each function is a function of a microcode address, by

only changing the value of control signals that are absolutely required for that particular microcode address (e.g., ADD, STORE, MULT etc. as determined by the decoding), the power of the microprocessor can be minimized since node toggle, as discussed above, is greatly reduced as compared to the conventional machines and systems (e.g., see specification at page 10, lines 6-11). That is, in an exemplary aspect of the claimed invention, each opcode becomes a function of the previous opcode and only conflicting (e.g., required) control signals must be resolved, thereby greatly reducing power consumption (e.g., see specification at page 10, lines 17-19).

With respect to independent claim 1, Applicants reiterate that independent claim 1 would not have been obvious from Damouny in view of Thoma.

For example, independent claim 1 recites, *inter alia*, a microprocessor, comprising:

> a microcode unit for outputting control signals, for each of a plurality of instructions, required by said microprocessor for executing said instructions, the microcode unit comprising:
>
> an instruction address input for receiving an instruction address;
> **a control variable input** for receiving a control variable corresponding to **a current state** of the microprocessor;
> **a control signal input** for receiving **all the control signals output** by the microcode unit **for an immediately preceding instruction**; and
> a plurality of embedded logic circuits each dedicated for evaluating one unique type of instruction received by the microcode unit and for setting the control signals **required** for executing said received instruction (emphasis added).

Applicants submits that it would not have been obvious to modify Damouny in view of Thoma since, by teaching that every control signal is modified for each instruction, Damouny would teach away from the claimed invention. Moreover, if Damouny were modified to arrive at

the claimed invention, such a modification clearly would require a change in the principle of operation of the device of Damouny.

Applicants also reiterate that dependent claims 2-4 and 6 also should be patentable at least by virtue of their dependency from claim 1, as well as for the additional recitations recited therein.

For example, with respect to claim 3, in the Response to Arguments, the Examiner alleges that "*[t]he third limitation has been given patentable weight counter to what the Applicant thought was the examiner's intention and the examiner had wished only to point out that regarding the first two limitations, the phrase "regardless of the preceding value" is inherently met since the signals will be either set based on the previous value or not based on the value. Regarding the third limitation, when the control signal of mention does not change from one instance to the next, the control signal is set to the same value as before and is not modified from the previous value, but is modified to retain the value*" (see Office Action at page 14, numbered paragraph 26; emphasis original).

Dependent claim 3 recites, *inter alia*, that the controller includes:

> means for setting a control signal to a "1" regardless of its immediately preceding value;
> means for setting a control signal to a "0" regardless of its immediately preceding value; and
> means for not modifying a control signal from its immediately preceding value (emphasis added).

The specification clearly describes that, in addition to the "0" or "1" value which can be set for each control signal, the previous value can also be set, thereby reducing the power within the microprocessor (e.g., see specification at page 10, lines 2-5).

As mentioned above, the Examiner alleges that "*when the control signal of mention does not change from one instance to the next, the control signal is set to the same value as before and is not modified from the previous value, but is modified to retain the value*".

However, Damouny and Thoma, alone or in combination, do not disclose or suggest maintaining and/or retaining the previous value. Instead, these references simply teach that every control signal is modified for each instruction.

Such clearly does not imply that Damouny or Thoma disclose "*means for not modifying a control signal from its immediately preceding value*" as claimed. Indeed, the Examiner has not cited any structure, equivalents thereof, or identity of function necessary for the claimed "*means for not modifying a control signal from its immediately preceding value*".

Thus, Applicants respectfully submit that claim 3 is patentable over Damouny and Thoma, either alone or in combination.

With respect to claim 6, in the Response to Arguments, the Examiner alleges that "*Applicant has argued that since Damouny discloses that every control signal is modified for each instruction, no determination would need to be made on which control signals are to be modified and which are not to be modified. As Applicant has admitted, Damouny discloses automatically modifying every control signal for each instruction. This would then inherently mean that there is **means for determining** that **no** control signals are to **not** be modified since the system automatically modifies **all** control signals, whether the determination is hardwired and is the same determination every time or otherwise*" (see Office Action at page 15, numbered paragraph 27; emphasis added).

Applicants respectfully disagree with the Examiner's position, for several reasons.

Dependent claim 6 recites, *inter alia*, "means for determining which of the control signals are not to be modified for each instruction" (emphasis added).

To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency may not be established by probabilities and statistics. The mere fact that a certain thing may result from a given set of circumstances is not sufficient (see M.P.E.P. § 2112; see also *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999); emphasis added).

As mentioned above, Damouny discloses automatically modifying every control signal for each instruction. It would not be inherent in Damouny to provide a structural element which determines that "*no control signals are to not be modified*", as alleged by the Examiner, simply because the system automatically modifies all control signals.

On the contrary, since all control signals in Damouny are automatically modified, there is no need (i.e., it is not necessary) to even make such a determination. As mentioned above, inherency requires that the missing element **necessarily** flows from the teachings of the applied art.

Damouny clearly does not necessarily disclose or suggest making such a determination, or for that matter, any structural features which would make such a determination. Indeed, the Examiner has not cited any structure, equivalents thereof, or identity of function necessary for the claimed "means for determining".

Moreover, Damouny does not, and cannot, modify some (i.e., not all) of the control signals. Thus, it clearly is unreasonable to interpret Damouny as inherently including a feature which it does not need to perform (or cannot perform).

Applicants also submit that it clearly is unreasonable to interpret Damouny as inherently including the claimed feature even though it has no use for such a feature. In fact, if Damouny were modified to include such features, such modifications would change the principle of operation of the Damouny reference.

For the foregoing reasons, Applicants respectfully submit that Damouny and Thoma, either alone or in combination, do not disclose or suggest all of the features of claim 6.

With respect to newly added claims 23-30, the Examiner rejects these claims as being unpatentable over Damouny in view of Thoma. However, Applicants respectfully submit that claims 23-30 would not have been obvious from Damouny and Thoma, alone or in combination. Therefore, Applicants traverse the rejection of these claims.

For example, dependent claim 24 recites, *inter alia*, that "each of the plurality of embedded logic circuits comprises a controller for controllably setting only each of the control signals required by the microprocessor for executing said received instruction" (emphasis added).

The Examiner alleges that Figure 1A of Damouny discloses this feature of the claimed invention. However, as the Examiner also acknowledged in the Office Action mailed on April 16, 2004, and in the present Office Action, Damouny discloses that "*every control signal is modified for each instruction*".

Thus, Damouny clearly does not disclose or suggest "a controller for controllably setting only each of the control signals required by the microprocessor for executing said received instruction" as claimed.

As another example, dependent claim 27 recites, *inter alia*, that "the controller includes means for maintaining a control signal at an immediately preceding value of said control signal" (emphasis added).

However, as mentioned above, Damouny and Thoma, alone or in combination, do not disclose or suggest maintaining and/or retaining the previous value.

Instead, the references simply teach that every control signal is modified for each instruction. Such clearly does not imply that Damouny or Thoma disclose "*means for maintaining a control signal at an immediately preceding value of said control signal*" as claimed.

Indeed, the Examiner has not cited any structure, equivalents thereof, or identity of function necessary for the claimed "*means for maintaining a control signal at an immediately preceding value of said control signal*".

Thus, Applicants respectfully submit that claim 27 is patentable over Damouny and Thoma, either alone or in combination.

On the other hand, dependent claim 30 recites, *inter alia*, "means for determining at least one of said control signals to be maintained for each instruction" (emphasis added).

However, as mentioned above, Damouny and Thoma, alone or in combination, do not disclose or suggest maintaining and/or retaining the previous value.

Instead, the references simply teach that every control signal is modified for each instruction. Such clearly does not imply that Damouny or Thoma disclose "*means for determining*" as claimed.

Indeed, the Examiner has not cited any structure, equivalents thereof, or identity of function necessary for the claimed "*means for determining*".

Thus, Applicants respectfully submit that claim 30 is patentable over Damouny and Thoma, either alone or in combination.

For the foregoing reasons (and the reasons set forth in the Amendment under 37 C.F.R. § 1.111 filed on July 16, 2004, which are incorporated herein by reference in their entirety), Applicants respectfully submit that Damouny and Thoma, either alone or in combination, do not disclose or suggest all of the features of the claimed invention.

Therefore, the Examiner respectfully is requested to reconsider and withdraw the rejection of these claims and permit claims 1-4, 6, 9, 20, and 23-30 to pass to immediate allowance.

III. CONCLUSION

In view of the foregoing, Applicants submit that claims 1-4, 6, 9, 20, and 23-30, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 09-0456.

Respectfully Submitted,

Date: December 13, 2004

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CERTIFICATE OF TRANSMISSION

I certify that I transmitted via facsimile to (703) 872-9306 the enclosed Amendment under 37 C.F.R. § 1.116 to Examiner Shane F. Gerstl on December 13, 2004.

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